5

1. In a semiconductor device wherein conductive interconnection members are What is claimed is: inlaid into and separated at a surface by a dilectric member, the spacing of said 1 conductive interconnection members at said surface being in the sub 250 nanometer range, and said conductive interconnection members exhibiting high electric field concentrations at said surface, 5 an improvement comprising: a mask member extending over all of said dielectric member from a first 6 conductive interconnection member to a second conductive interconnection 7 8 said mask member being positioned in contact with said dielectric member 9 and intersecting said conductive interconnection members at a location 10 11 that is separated from said surface. 12 2. The improvement of claim 1 wherein the material of said conductive interconnection members is at least one member of the group comprising copper, 1 2 aluminum, silver, gold and alloys thereof. 3 3. The improvement of claim 2 wherein the material of said mask member is a at least one material taken from the group of amorphous silicon, carbon, hydrogen 1 ( & - Si:CH); silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:OH); 2 silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride(Si<sub>3</sub>N<sub>y</sub>); silicon dioxide(Si O<sub>2</sub>); 3 4 and, silicon oxynitride (SiON).

- 4. The improvement of claim 1 wherein said mask member has a thickness related 1
- to the capacitance of said conductive interconnect members. 2
- 5. The improvement of claim 1 wherein said location of said mask member 1
- intersecting with said conductive interconnect members is separated from said 2
- surface a distance in the range of 1 to 20 nanometers. 3
- 6. The improvement of claim 5 wherein said location of said mask member 1
- intersecting said conductive interconnect members is separated from said surface 2
- a distance of 5 nanometers. 3
- 7. The improvement of claim 6 wherein said conductive interconnect members in 1
- said dielectric member are surrounded by an electrically conductive diffusion 2
- barrier liner. 3
- 8. The improvement of claim 7 wherein said liner is of a material taken from the 1
- group of at least one of Ta, Ti, TaN, TiN, W and WN. 2
- 9. A semiconductor device wherein conductive interconnection 1
- members are inlaid into and separated at a surface of a bulk dielectric member, the 2
- spacing of said conductive interconnection members at said surface being in the sub 3
- 250 nanometer range, and said conductive interconnection members exhibiting high 4
- electric field concentrations at said surface, 5
- an improvement comprising: 6

| YOR92 | 000333US1 13 of amorphous silicon,   |
|-------|--|
| _     | a mask member of at least one material taken from the group of amorphous silicon,  |
| 7     | a mask member of the state of t |
| 8     | (organosilozana or Si:C:O:H); silicon, nitrogen, carbon alloys (Si:N:C); silicon   |
| 9     | (organosilozane or Si:C:O:H); salcon, mitogar, extending   |
| 10    | (organosiloxans of Si-O-O-), and , silicon oxynitride (SiON); extending nitride (Si <sub>3</sub> N <sub>F</sub> ); silicon dioxide (Si O <sub>2</sub> ); and , silicon oxynitride (SiON);  |
| 10    | over all of said dielectric member from a first conductive interconnection   |
| 11    | member to a second conductive interconnection member,  |
| 12    | member to a second conductive interest and the material taken from   |
| 13    | said conductive interconnect members being of at least one material taken from   |
|       | the group of copper, aluminum, silver, gold and alloys thereof.  |
| 14    | said mask member being positioned in contact with said dielectric member   |
| 15    | said mask member being position  |
| 16    | and intersecting said conductive interconnection members at a location   |
| 17    | that is separated from said surface.   |
| 1,    |  |
| 1     | 10. The device of claim 9 wherein conductive interconnect members in   |
| 1     | said bulk polymer member are surrounded by an electrically conductive  |
| 2     | said bulk paryuna manara and an  |
| 3     | diffusion barrier liner.   |
|       | the state of a material taken from the   |
| 1     | 11. The device of claim 9 wherein said liner is of a material taken from the   |
| •     | group of at least one of Ta, Ti, TaN, TiN, W and WN.   |
| 2     |  |
| _     | 12. A semiconductor device wherein conductive interconnection members are  |
| 1     | inlaid into and separated at a surface of a bulk dielectric member, the spacing of said  |
| 2     | inlaid into and separated at a summer of the sub 250 nanometer   |
| 3     | conductive interconnection members at said surface being in the sub 250 nanometer  |
| 4     | range, and said conductive interconnection members exhibiting high electric field  |
| 5     | concentrations at said surface,  |

| YOR92 | 0000333US1        | 14                     |  |
|-------|-------------------|------------------------|--|
| 6     | an improvement co | imprising:             | rs being of at least one material taken from   |
| 7     |                   | a Comments             | diva. Some   |
| 8     | the group of      | f copper, aluminum     | ars extending above the surface of said  |
| 9     | said conductive   | interconnect menna     | in the range of from 1 - 20 nanometers.  |
| 10    | intralevel        | dielectric a distance  | in the second connect  |
| 1     | 13. The device    | of claim 12 wherein    | said distance said conductive interconnect   |
| 2     | members exte      | nd above said surfac   | e of said intralevel dielectric is from 2 - 5  |
| 3     | nanometers.       |                        |  |
| 1     | 14 The proc       | ess of preventing hi   | igh electric field concentration in a  |
| 2     | surface of a di   | electric body at a far | cetted shaped intersection with sub 250 conductive interconnect members in said body,  |
| 3     |                   |                        |  |
| 4     | comprising        | _                      | material that is hardened relative to the hardness   |
| :     |                   |                        | -ding at least the   |
|       |                   | - Ci                   | dielectric member  |
|       | 7 over at 1       | east a portion or sai  | y the beginning of said facetted portion.  |
|       | 8 surface         | a distance defined t   | y and member is a  |
|       | 1 15. The 1       | process of claim 14    | wherein the material of said mask member is a  p of amorphous silicon, carbon, hydrogen (cc. Si:C:H);  (compansiloxane or Si:C:O:H); silicon, nitrogen |
|       | 2 material        | taken from the grou    | gen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen<br>sen alloys (organosiloxane or Si:C:O:H); silicon, nitrogen                               |
|       | 3 silicon, o      | arbon, oxygen, nyuru   | gen alloys (organisation of a silicon of a silicon on nitride (Si $_2$ ); and , silicon on nitride (Si $_3$ N $_4$ ); silicon of a silicon             |
|       |                   |                        |  |
|       | 5 oxynit          | ride (SiON).           |  |

- 16. In a process of fabricating sub 250 nanometer size and spacing semiconductor 1
- device interconnections wherein conductive interconnect members pass through a
- portion of a bulk dielectric to a common surface, 2 3
- an improvement comprising the intermediate steps of:
- depositing a diffusion barrier liner in the formation of said conductive interconnect
- members where said conductive interconnect members pass through said bulk 6
- dielectric, and then, employing said diffusion barrier liner as the conductor for 7
- plating in subsequent deposition of metal filling said conductive interconnect 8
- members. 9
  - 17. The process improvement of claim 16 wherein the material of said diffusion
- barrier liner is a material taken from the group of at least one of Ta, Ti, TaN, TiN, W 1
- and WN, and said subsequently deposited metal is copper.. 3
- 18. The process of fabricating sub 250 nanometer size and spacing semiconductor 1
- device interconnections wherein conductive interconnect members pass through a
- portion of a bulk dielectric body and through a mask layer atop said dielectric to a
- common surface,
- the improvement comprising the intermediate steps of: 5
- etching trench and via shape openings out of said dielectric body through said mask 6
- layer in a region below said surface, 7
- lining said openings with thin electrically conductive diffusion barrier layer, 8

- coating said liner layer with a thin metal layer, 9
- electroplating a thick metal into and filling said openings including overcoating said 10
- 11
- planarizing said overcoated surface through chemical mechanical operations, and, 12
- removing said mask layer in all portions between said openings to a depth that 13
- establishes a selected dimension of the upper surface of said mask below said 14
- surface. 15
- 19. The process of claim 18 wherein said mask layer is of at least one material 1
- taken from the group of amorphous silicon, carbon, hydrogen (-c Si:CH); 2
- silicon, carbon, oxygen, hydrogen alloys (organosiloxane or Si:C:O:H); 3
- silicon, nitrogen, carbon alloys (Si:N:C); silicon nitride (Si3Ny); silicon dioxide (Si O2); 4
- and, silicon oxymitride (SiON). 5
- The process of claim 19 wherein said thin electrically conducting diffusion 1
- barrier layer is of at least one material taken from the group of Ta, Ti, TaN, TiN, W 2
- and WN, 3
- 21. The process of claim 20 wherein said thick metal being electroplated into 1
- and filling said openings is of at least one metal taken from the group of copper, 2
- aluminum, silver, gold and alloys thereof. 3